Docket No.: R2180.0188/P188
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Takamitsu Yamada et al.

Application No.: 10/763,255 Confirmation No.: 7512

Filed: January 26, 2004 Art Unit: 2117

For: SEMICONDUCTOR INTEGRATED CIRCUIT AND SCAN TEST METHOD THEREFOR Examiner: Phung M. Chung

AMENDMENT AFTER FINAL OFFICE ACTION UNDER 37 C.F.R. 1.116

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

In response to the Office Action dated May 21, 2007, finally rejecting claims 1, 2, 7, 12-15 and 25-30, please amend the above-identified U.S. patent application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 7 of this paper.